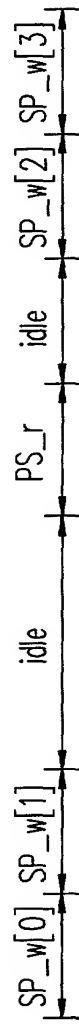


FIG. 1 (PRIOR ART)



Secondary bus(Label S)



Primary bus(Label P)

*PS_r_a: address phase of the PS_r
 *PS_r_d: data phase of the PS_r
 *SP_w[3:0]: posted write cycle

FIG. 2 (PRIOR ART)

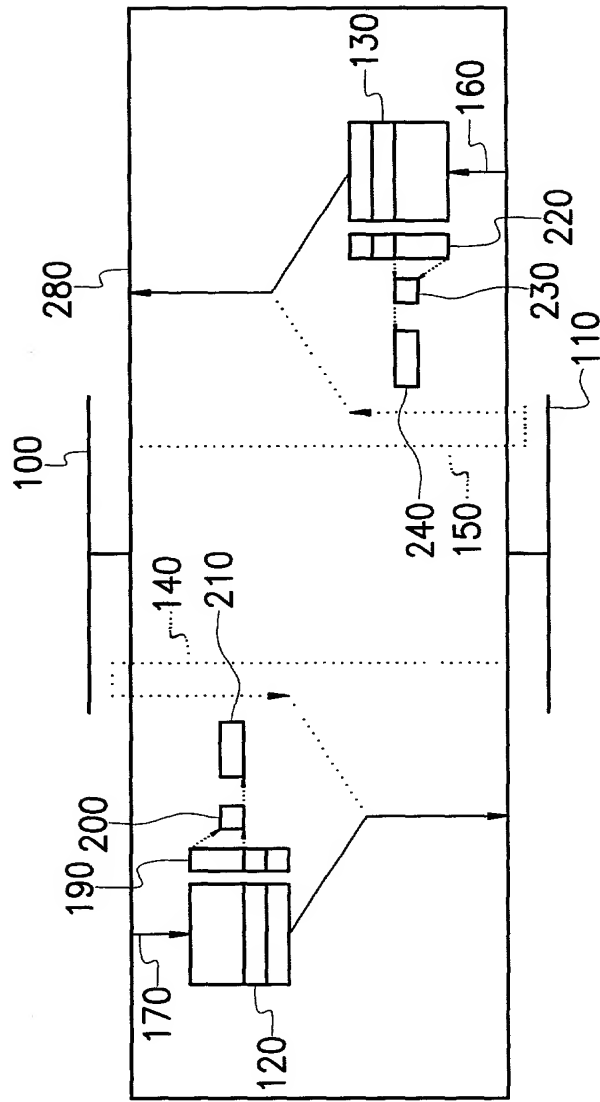


FIG. 3

Secondary bus(Label S) $SP_w[0]$ $SP_w[1]$ PS_r $SP_w[2]$ $SP_w[3]$

Primary bus(Label P) PS_r_a $SP_w[0]$ $SP_w[1]$ PS_r_d

*PS_r_a: address phase of the PS_r
 *PS_r_d: data phase of the PS_r
 *SP_w[3:0]: posted write cycle

FIG. 4